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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/575,819	04/13/2006	Seong-Young Lee	AB-1867 US	5258

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MACPHERSON KWOK CHEN & HEID LLP
2033 GATEWAY PLACE
SUITE 400
SAN JOSE, CA 95110

EXAMINER	
SALERNO, SARAH KATE	

ART UNIT	PAPER NUMBER
2814	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/575,819	LEE ET AL.	
	Examiner	Art Unit	
	SARAH K. SALERNO	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 January 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14,16-22,24 and 25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14,16-22,24 and 25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's amendment/arguments filed on 01/16/08 as being acknowledged and entered. By this amendment claims 15 & 23 are canceled, no new claims have been added and claims 1-14, 16-22 and 24-25 are pending.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-6, 9-14, 16-17,19-22 & 24-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kubo et al. (US Patent 6,091,467) in view of Kubota et al. (JP Pub # 10-098190).

Claim 1: Kubo teaches a thin film transistor comprising (FIG. 13): a gate electrode (201); a gate insulating layer (202) formed on the gate electrode (201); a semiconductor layer (203-205) formed on the gate insulating layer (202) and disposed opposite the gate electrode (201); a source electrode (206) and a drain electrode (207) that are formed at least in part on the semiconductor layer (203-205) and face each other; a passivation layer (208) formed on the source electrode (206), the drain electrode (207), and a portion of the semiconductor layer (203-205) that is not covered with the source electrode (206) and the drain electrode (207); and a shielding electrode

(210) formed on the passivation layer (208) and disposed on a region between the source electrode (206) and the drain electrode (207).

Kubo does not teach the shielding electrode providing voltage shielding fro the region on which it is disposed. Kubota teaches a shielding electrode providing voltage shielding for the region on which it is disposed (Abstract) improving the characteristics of the thin-film transistor. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the shielding electrode taught by Kubo with the one taught by Kubota to improve the characteristics of the thin-film transistor (Abstract) as taught by Kubota.

Claim 6: Kubo teaches the shielding electrode comprises IZO or ITO (Col. 11 lines 13-25)

Claim 9: Kubo teaches a thin film transistor array panel comprising: a gate line and a data tie line; a first thin film transistor including a control electrode, an input electrode, an output electrode, and a channel portion disposed between the input electrode and the output electrode and generating a gate signal to be applied to the gate line; a second thin film transistor including a gate electrode connected to the gate line, a source electrode connected to the data line, a drain electrode, and a channel portion disposed between the source electrode and the drain electrode and transmitting a data signal from the data line in response to the gate signal from the gate line; a pixel electrode connected to the drain electrode to receive the data signal; and a first shielding electrode disposed on the channel portion of the first thin film transistor

wherein the first shielding electrode is formed of the same laver as the pixel electrode (Description of the Related Art; Figs. 9-10, 12).

Claims 2 & 10: Kubo teaches the shielding electrode is electrically isolated (FIG. 13).

Claim 3 & 11: Kubota teaches a shielding electrode is supplied with a predetermined voltage to prevent the accumulation of electric charge on the light-shield film [0018, 0039]. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the device taught by Kubo to supply the shielding electrode with a predetermined voltage to prevent the accumulation of electric charge on the light-shield film as taught by Kubota [0018,0039].

Claims 4 & 12: Kubota teaches the predetermined voltage supplied to the shielding electrode is equal to or lower than a ground voltage [0039].

Claims 5 & 13: Kubota teaches the predetermined voltage supplied to the shielding electrode is a negative voltage [0039].

Claim 16: Kubo teaches a second shielding electrode disposed on the channel portions of the second thin film transistor and including the same layer as the pixel electrode (Description of the Related Art; Figs. 9-10, 12).

Claim 17: Kubo teaches an insulating layer disposed between the first and the second thin film transistors and the first and the second shielding electrodes (Description of the Related Art; Figs. 9-10, 12).

Claim 19: Kubo teaches a display device comprising: a gate line and a data line; a first thin film transistor including a channel portion and generating a gate signal to be

applied to the gate line; a second thin film transistor transmitting a data signal from the data line in response to the gate signal from the gate line; a pixel electrode connected to the second thin film transistor to receive the data signal; a shielding electrode disposed on the channel portion of the first thin film transistor wherein the shielding electrode is formed of the same layer as the pixel electrode; and a common electrode facing the pixel electrode (Description of the Related Art; Figs. 9-10, 12).

Claim 20: Kubo teaches the shielding electrode faces, the common electrode (FIG. 12).

Claim 21: Kubota teaches the shielding electrode is supplied with a predetermined voltage lower than a voltage applied to the common electrode [0004, 0013, 0018-0019, 0022, 0050-0059].

Claims 14 & 22: Kubota teaches the predetermined voltage supplied to the first shielding electrode has a magnitude for turning of the second thin film transistor [0004, 0013, 0018-0019, 0022, 0050-0059].

Claim 24: Kubo teaches a dielectric layer (216) disposed between the shielding electrode and the common electrode (FIG. 12).

Claim 25: Kubo teaches the dielectric layer (216) comprises a liquid crystal layer (col. 2 lines 10-20).

4. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kubo et al. (US Patent 6,091,467) and Kubota et al. (JP Pub # 10-098190), as applied to claim 1 above, and further in view of Tsubo (US PGPub 2002/0057396)

Regarding claim 7, as described above, Kubo and Kubota substantially reads on the invention as claimed, except Kubo and Kubota do not teach the shielding electrode has a shape of horseshoes. Tsubo teaches a U-shape shielding electrode which reduces the variance in parasitic capacitance of the device [0061, 0072]. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the shield electrode taught by Ikeda to be a U-shape to increase the performance of the device as taught by Tsubo [0061, 0072].

5. Claims 8 & 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kubo et al. (US Patent 6,091,467) and Kubota et al. (JP Pub # 10-098190) as evidenced by Kawasaki et al. (US Patent 6,281,552) (col. 8 lines 44-50).

Claims 8 & 18: Kubo teaches the passivation layer (108/208) comprises an acrylic resin which is said to be an organic insulator (Col. 1 lines 60-67) as evidenced by Kawasaki (col. 8 lines 44-50).

Response to Arguments

6. Applicant's arguments with respect to claims 1-8 have been considered but are moot in view of the new ground(s) of rejection. The combination of Kubo and Kubota teach shielding electrodes which provide voltage shielding for the region on which it is disposed as described above in the rejection of claim 1.

7. Applicant's arguments filed 01/16/08 have been fully considered but they are not persuasive.

Applicant argues that Kubo fails to teach the shielding electrode comprising IZO or ITO. This argument is not persuasive because the passage cited from Kubo in the previous office action teaches a light shielding film made of ITO (Col. 11 lines 15-16 & 19).

Applicant argues that Kubo does not disclose all of the limitations of claim 9 & 19 and that Kubo discloses only light shielding and then only light shielding for thin film transistors in the lighted portion of a display. Applicant's arguments are not persuasive because the claim language does not require what type of shielding is performed by the electrode or which portion of the device is shielded. Kubo teaches all the limitation of claim 9 & 19 as described in the above rejection using figures 9-10 & 12 and Col. 1-2 including first and second thin film transistors, the channel of the first generating a gate signal to be applied to the gate line and the second including a gate electrode connected to the gate line. It is noted that where the claimed and prior art products are identical or substantially identical in structure or composition or are produced by identical or substantially identical processes, claimed properties or functions are

presumed to be inherent. In re Best, 195 USPQ 430, 433 (CCPA 1977). It has also been held that products of identical chemical composition cannot have mutually exclusive properties. A chemical composition and its properties are inseparable. Therefore, if the prior arts teach the identical chemical structure the properties applicant discloses and/or claims are necessarily present. In re Spada, 15 USPQ 2d 1655, 1658 (Fed. Cir. 1990). In this case the TFT's taught by Kubo would inherently have the property of being able to generate a gate signal to be applied to the gate line, because the TFTs are structured as claimed.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SARAH K. SALERNO whose telephone number is (571)270-1266. The examiner can normally be reached on M-R 7:30-5:00pm every other F 7:30-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/S. K. S./
Examiner, Art Unit 2814

/Theresa T. Doan/
Primary Examiner, Art Unit 2814